Abstract of the Disclosure

A timing loop controller for multilevel modulation scheme is disclosed. The timing loop controller includes a first to fourth computing unit for computing a timing error between an input timing of digital signals and a sampling timing; a first to fourth quantization unit for controlling a direction and an error value of the timing error; a first and second sign detection unit for detecting sign change according to results; a zero crossing detection unit for detecting zero crossing at I axis and Q axis; and a timing error control unit for controlling the timing error value in case there is no sign change. The present invention can increase a zitter performance of timing error according to the signal-to-noise ratio by detecting the timing error, outputting the timing error and controlling the timing error output value only in case there is sign change by additionally equipping the sign variation detector.